REMARKS

Reconsideration of this application, as amended, is respectfully requested.

THE TITLE

The title has been amended to more clearly indicate the nature of the invention to which the claims are directed.

THE CLAIMS

The claims have been amended to make some minor clarifications so as to more clearly recite the distinguishing features of the present invention. In particular, it is noted that claim 1 has been amended to clarify that the plurality of columnar electrodes each have "an upper edge surface outwardly exposed" for connection to an external "device", and that the sealing film covers the thin film passive element and the semiconductor substrate except for the upper edge surface of each of the columnar electrodes. Claims 4 and 5 have been amended to clarify that the two portions included in the at least one conductive layer have opposing end surfaces. Claim 13 has been amended to correct a minor clerical error. Independent claim 14 has been amended to clarify that the columnar electrodes are provided for connection to an external "device", that the sealing film is formed on "an exposed entire upper surface of the

semiconductor wafer substrate, and that only an upper edge surface of each of the columnar electrodes is exposed from the sealing film. And claims 17 and 18 have been amended to clarify that the two portions of the conductive layer formed on the insulating film have opposing end surfaces.

It is respectfully submitted that the amendments to the claims are clarifying in nature only and that no new issues have been raised which require further consideration on the merits and/or a new search. Accordingly, it is respectfully requested that the amendments to the claims be approved and entered under 37 CFR 1.116.

THE PRIOR ART REJECTION

Claims 1-6, 9-11, 13-19 and 23-25 were rejected under 35 USC 103 as being obvious in view of the combination of USP 6,180,976 ("Roy") and USP 5,258,886 ("Murayama et al"); claims 7 and 20 were rejected under 35 USC 103 as being obvious in view of the combination of Roy, Murayama et al and USP 6,002,161 ("Yamazaki"); and claims 8 and 21 were rejected under 35 USC 103 as being obvious in view of the combination of Roy, Murayama et al, Yamazaki and USP 6,331,722 ("Yamazaki et al"). These rejections, however, are respectfully traversed with respect to the claims as amended hereinabove.

The present invention relates to a chip size package (CSP) structure of a semiconductor device which comprises columnar electrodes for connection to an external device, on a semiconductor substrate where an integrated circuit is formed and connection pads for connection to the external device are formed. A sealing film is formed to cover the entire upper surface of a chip, except for the upper edge surfaces of the columnar electrodes, and the upper edge surfaces of the columnar electrodes serves as terminal portions for connection to the external device. Solder balls, for example, are provided on the upper surfaces of the columnar electrodes, and the columnar electrodes are electrically connected to, for example, electrodes of a wiring board of the external device through the solder balls.

Furthermore, in the chip size package of the semiconductor device of the present invention, a thin film passive element is stacked on the chip, as a result of which the provided circuit module has a smaller size.

To be more specific, the semiconductor device recited in the amended claim 1 comprises:

an organic insulating film formed on a circuit element-forming region of a semiconductor substrate which includes the circuit element-forming region and connection pads;

columnar electrodes electrically connected to the connection pads, and each including an upper edge surface outwardly exposed for connection to an external device;

a thin film passive element including at least one conductive layer formed on the insulating film; and

a sealing film formed to cover the entire upper surface of the semiconductor substrate, except for the upper edge surfaces of the columnar electrodes.

The semiconductor substrate of the present invention as recited in amended claim 13, moreover, includes a number of thin film passive elements.

In addition, the claimed present invention includes a method of manufacturing a semiconductor substrate as recited in amended claim 14 which comprises:

forming an organic insulating film on a circuit element-forming region of a semiconductor substrate which includes the circuit element-forming region and connection pads, and also forming a thin film passive element including at least one conductive layer on the insulating film;

forming columnar electrodes which are provided for connection to an external device, and which are electrically connected to the connection pads;

forming a sealing film such that the sealing film covers the entire upper surface of the semiconductor substrate;

exposing only an upper edge surface of each of the columnar electrodes from the sealing film; and

dividing a semiconductor wafer substrate into individual chip forming regions so as to form a plurality of semiconductor devices including respective thin film passive elements.

Furthermore, according to the present invention as recited in amended claim 4, the thin film passive element is a capacitance element, and the capacitance element comprises a conductive layer which includes two portions having opposing end surfaces and formed in one layer on the insulating film, with a dielectric material layer formed in a clearance between the opposing end surfaces of the two portions.

Similarly, according to the present invention as recited in amended claim 17, forming the thin film passive elements comprises forming at least one capacitance element, and the capacitance element is formed by forming, on the insulating film, a conductive layer including two portions having opposing end surfaces, and by forming a dielectric material layer in a clearance between the opposing end surfaces of the two portions of the conductive film.

Still further, according to the present invention as recited in amended claim 5, the thin film passive element is a capacitance element, and the conductive layer of the capacitance element includes two portions having opposing end surfaces and

formed in one layer on the insulating layer, and columnar electrodes are formed as plate-like electrodes located opposite to each other with a dielectric material layer formed in a clearance between the opposing end surfaces of the plate-like electrodes.

And similarly, according to the present invention as recited in amended claim 18, forming the thin film passive elements comprises forming at least one capacitance element, and the capacitance element is formed by forming a conductive layer having opposing end surfaces, on the insulating film, and by forming the columnar electrodes as plate-like electrodes on the two portions of the conductive layer and forming a dielectric material layer in a clearance between the plate-like electrodes. By this method, in the capacitance element, the end surfaces of the conductive layer or the opposing surfaces of the plate-like electrodes formed on the conductive layer substantially serve as the electrodes of the capacitance element, as a result of which the plane size of the capacitance element is reduced, and the dimension of the circuit module is also reduced.

In contrast to the present invention as recited in amended claims 1, 13 and 14, Roy discloses a structure comprising a capacitor 500 which includes an insulating film 26 formed on a wafer, an electrode (plate) 504 and an electrode (base plate) 506 stacked on the insulating film 26, and a dielectric material

layer 508 formed between the electrodes, lines 502, 503, 518, 520, 532, 534, 536 and 538, and conductor plugs 510, 512, 514 and 516, as shown in Fig. 13. In such a manner, reference numerals 502, 503, 518, 520, 532, 534, 536 and 538 denote lines, with their cross sections shown in Fig. 13. It is respectfully submitted, however, that none of Figs. 1-17 of Roy show connections pads for connection to an external device. Roy merely discloses a part of an integrated circuit including a number of lines and a capacitor. Accordingly, it is respectfully submitted that the structure disclosed in Roy is entirely different from the structure of the chip size package of the present invention.

In addition, it is respectfully pointed out that the capacitor 500 of Roy has two conductive layers. In this regard, the capacitor 500 corresponds to the thin film passive element of the present invention which includes at least one conductive layer. However, the thin film passive element of the present invention is formed on the organic insulating film formed on the circuit element-forming region, whereas the insulating film 26 included in the capacitor 500 in Roy merely has doped or undoped silicon oxide, phosphosilicate glass, tetrathylorbosilane, low-k dielectric materials. (See Roy at column 6, lines 44-48.) Thus, Roy does not disclose, teach or suggest that the insulating film serves as an organic insulating film.

Newly cited Murayama et al discloses a structure wherein a hybrid dielectric thin film is provided between a pair of electrodes constituting a capacitor, and comprises a first region and a second region formed of auxiliary material and incorporated into the first region, and material containing organic matter is used as the auxiliary material. It is respectfully pointed out, however, that the hybrid dielectric thin film of Murayama et al is provided between the pair of electrodes, and is simply used as the auxiliary material of which the hybrid dielectric thin film is formed. Accordingly, even if Roy and Murayama et al were combinable in the manner suggested by the Examiner, the combination of these references still would not suggest that the insulating film serves as an organic insulating film.

Still further, it is respectfully pointed out that the conductor plugs 512 and 513 in Fig. 13 of Roy are merely connected between the lines 502 and 503 and the lines 532 and 538. (See Roy at column 10, lines 5467, and column 11, lines 38-55.) In such a manner, the lines 502, 503, 532 and 538 of Roy are not connection pads, nor are their upper edge surfaces exposed. By contrast, according to the claimed present invention, the columnar electrodes are electrically connected to connection pads for connection to an external device, and their upper edge surfaces are exposed to the outside and used for

connection to the external device. The columnar electrodes therefore clearly differ from the conductor plugs of Roy.

In addition, it is respectfully pointed out that the insulating material 530 in Fig. 13 of Roy is provided between the lines 502 and 503 and the conductor plugs 512 and 513, and also covers the capacitor 500. By contrast, the sealing film of the claimed present invention covers the thin film passive element, and is provided between the columnar electrodes. And it is also noted that the sealing film of the claimed present invention covers the entire upper surface of the semiconductor substrate, except for the upper edge surfaces of the columnar electrodes.

Therefore, since the conductor plugs of Roy do not correspond to the columnar electrodes of the claimed present invention, as stated above, the insulating material 530 of Roy also does not correspond to the sealing film of the claimed present invention.

In view of the foregoing, it is respectfully submitted that the structures of the present invention as recited in claims 1, 13 and 14 of the present application are not at all disclosed, taught or suggested by the combination of Roy and Murayama et al.

With respect to the structure of the present invention as recited in claims 2 and 15 of the present application, moreover, it is noted that Roy discloses that a capacitor is formed on a wafer, with an insulating film 26 interposed therebetween. This

structure corresponds to a structure wherein the thin film passive element is a capacitance element in the present invention. It is respectfully submitted, however, that the structures of claims 2 and 15 cannot be derived from Roy or Murayama et al, since they depend on claims 1 and 14, respectively, which are not rendered obvious by the combination of these references.

Fig. 12 of Roy discloses that a capacitor 400 is formed to comprise an upper electrode (top plate) 402 and a lower electrode (bottom plate) 404 which are stacked on the wafer, with the insulating film 26 interposed therebetween, and a dielectric material layer provided between the electrodes. The structure wherein the stacked electrodes and the dielectric material layer provided therebetween constitute a capacitor corresponds to a structure in each of claims 3 and 16, wherein two conductive layers are stacked, and a dielectric material layer is provided between the conductive layers. However, the structure taught in each of claims 3 and 16 cannot be derived from Roy or Murayama, since these claims also depend from claims 1 and 14, respectively, which are not rendered obvious by the combination of these references.

Also, Fig. 12 of Roy discloses that, as stated above, the capacitor 400 comprises the upper electrode (top plate) 402, the lower electrode (bottom plate) 404 and the dielectric material

layer provided between the electrodes, and further that a conductor plug 414 is connected to the upper electrode 402, a conductor plug 416 is connected to the lower electrode 404, and an insulating layer 406 is formed between a conductor plug 418 and lines 408, 410 and 412. However, it should be noted that the upper electrode 404 and lower electrode 506 included in the capacitor 400 are stacked opposite to each other in the vertical direction, with the insulating layer 406 interposed therebetween; i.e., they are not formed in the same layer, unlike as according to the present invention as recited in claims 4 and 17. In addition, it is also respectfully submitted that Roy clearly does not disclose a structure wherein the end surfaces of the conductive layer are located opposite to each other. That is, Roy discloses no structural element corresponding to the conductive layer of the claimed present invention which has at least two portions having opposing end surfaces. Thus, Roy does not suggest the structural feature of the claimed present invention whereby a dielectric material layer is formed in a clearance between the opposing end surfaces of the conductive layer, as recited in claims 4 and 17.

As repeatedly stated above, Fig. 12 of Roy merely discloses that the capacitor 400 comprises the upper electrode (top plate) 402 and the lower electrode (bottom plate) 404. It is obvious that Roy does not disclose a structure in which the end surfaces

of the conductive layer which are formed in the same layer are located opposite to each other, unlike as according to the present invention as recited in claims 5 and 18. That is, Roy discloses no structural element corresponding to the conductive layer of the claimed present invention which has at least two portions having opposing end surfaces. Also, Roy discloses no structural element corresponding to the columnar electrodes formed opposite to each other on the two portions, respectively. Thus, Roy does not suggest the structural feature of the claimed present invention whereby a capacitor is formed such that a dielectric material layer is formed in a clearance between the columnar electrodes, as recited in claims 5 and 18.

With respect to the structure recited in claims 6 and 19, moreover, Roy simply discloses that an inductor may be formed on the wafer. In addition, it is noted that claims 6 and 19 depend on claims 1 and 14, respectively, which are not rendered obvious by the combination of these references. Accordingly, it is respectfully submitted that the structure in each of claims 6 and 19 is also not suggested in Roy or Murayama.

Still further, it is respectfully submitted that Roy does not disclose, teach or suggest the structure recited in each of claims 10, 11, 24 and 25, in which the terminals of the thin film passive element are connected to columnar electrodes or connection pads, since Roy does not disclose connection pads for

connection to an external device or columnar electrodes for use in connecting to the external device.

With respect to Yamazaki (USP No. 6,002,161) which was cited against claims 7 and 20, it is noted that this reference discloses a structure wherein a spiral conductive film pattern is formed on a semiconductor substrate, with an insulating film interposed therebetween, thereby forming an inductance element, which has two terminals. This corresponds to a structure wherein the thin film passive element is an inductance element. However, in addition to this feature, the present invention as recited in claims 7 and 20 has a further structural feature whereby at least one of two terminals of the inductance element is connected to at least one of a first connection pad not connected to any of the columnar electrodes and a second connection pad connected to at least one of the columnar electrodes. It is respectfully submitted that Yamazaki does not disclose any structural elements corresponding to the columnar electrodes and connection pads of the claimed present invention. And it is respectfully submitted that Roy and Murayama et al also do not disclose any structure corresponding to the columnar electrodes and connection pads of the claimed present invention. Accordingly, it is respectfully submitted that the structure of the present invention as recited in claims 7 and 20 cannot be achieved by the combination of Roy, Murayama et al and Yamazaki.

And finally, with respect to Yamazaki et al (USP 6,331,722) which was cited against claims 8 and 21, it is noted that this reference discloses a laminated device containing magnetic materials. This reference, however, does not disclose how the magnetic materials are provided in the laminated device. And accordingly, it is respectfully submitted that the feature of the present invention as recited in claims 8 and 21 wherein a magnetic film is formed on the conductive layer cannot be derived from Yamazaki et al.

In view of the foregoing, it is respectfully submitted that Roy, taken singly or with any of the other cited references, does not disclose, teach, or suggest the above-described features of the claimed present invention, and that all of the claims patentably distinguish over all of the cited references, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

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Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,

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